Minimizing Distortion in Operational Transconductance Amplifiers

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I. Introduction

The Operational Transconductance Amplifier (OTA) is perhaps one of the most indispensable circuits in analog music synthesis. It can be used to make VCOs, VCFs, VCAs, and a myriad other sound modifying devices. The reason for this, is that it is the simplest way to implement the mathematical function of multiplication. A simpler diode mixer or ring modulator could be used, but both are so horribly nonlinear that they are not really viable options. There are also true Gilbert-cell multipliers available which are better than OTAs, but they are an order of magnitude more expensive, making them prohibitive for DIY and large volume production

A colleague of mine once stated that if he could have only one IC to use, it would be the LM13700 (the most readily available OTA). The reason for this, is that it is not only a multiplier, but can also be wired as an op-amp, a variable current source, a variable resistor, a logarithmic current source, or any of the other applications shown in the extensive LM13700 datasheet. But, despite this versatility and subsequent ubiquity, the OTA has its shortcomings, and this paper will take a look at two of the worst: nonlinearity at high input levels and gain drift with temperature.

The OTA nonlinearity leads to a necessary trade-off between distortion and noise. The noise floor is fixed on an OTA for a given control current, so a smaller signal is closer to the noise floor, but is more linear. The temperature drift is a more subtle problem that is most apparent in frequency control circuits (like a VCF), as the ear is more sensitive to frequency than it is to amplitude. Luckily, both errors can be compensated for, and various methods of compensation will be analyzed and experimental results will be used to compare their relative merits.

II. Background

There are a number of different OTA topologies, ranging from the "diamond buffer" based OPA660 by Analog Devices to the voltage controlled current source of the MAX435 by Maxim. But, for this work, we will focus solely on the differential amplifier based topologies (e.g. CA3080), as these have the widest application in audio circuits due to their low cost and better linearity. In particular, the LM13700 (schematic symbol shown in Figure 1) will be used for most examples, as it is the only remaining OTA of its kind that is easily obtainable (the NE5517 is identical). It also comes in a dual package and has "linearizing diodes", and both of these qualities can be utilized to reduce distortion. Variants such as the LM13600 will be lumped together with the LM13700, as the only difference is the output buffer, and output buffers will not be analyzed in this work.

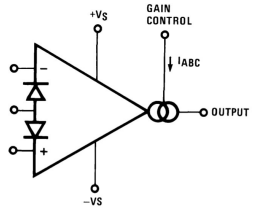

Fig. 1. OTA schematic symbol, with linearizing diodes.

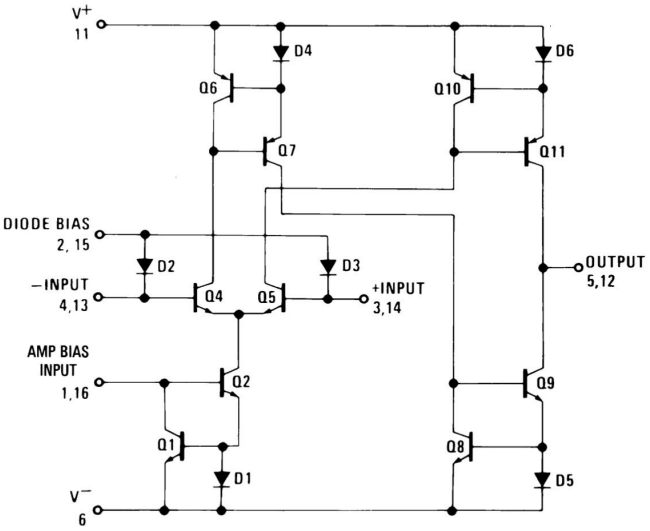

Fig. 2. Internal transistor configuration of the LM13700 (from the Texas Instruments datasheet).

As shown in the internal wiring diagram of Figure 2, the core of the LM13700 is a differential amplifier (Q4, and Q5). As a result, a basic OTA can be made with just two transistors, and is a good starting point for understanding OTA operation. An example of this is shown in Figure 3, where a control current is pulled through the emitters of the two transistors, and the difference between their collector currents is the output. A differential input signal is applied to the bases of the transistors, moving current between the halves of the differential pair.

The relationship between these inputs and the output can be found by using the Bipolar Junction Transistor (BJT) transfer function:

$$I_c = I_s \cdot e^{V_{be}/V_t} \rightarrow V_{be} = V_t \cdot \ln(I_c/I_s), \qquad (1)$$

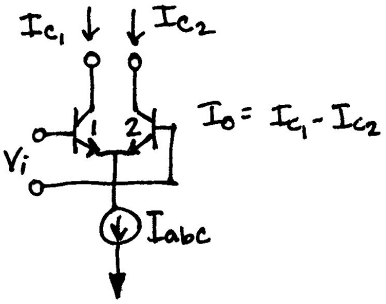

Fig. 3. Differential pair OTA core.

where I_c is the collector current, I_s is a device specific parameter, V_{be} is the voltage between the base and emitter, and V_t is the "thermal voltage" ($\sim$26mV). If we neglect base currents, we can say that emitter currents equal collector currents, and therefore the sum of the collector currents must equal the control current ($I_{c1} + I_{c2} \approx I_{abc}$). Since the input is just the difference in V_{be}, and assuming we have a "matched pair" of transistors with identical I_s and V_t values, we get:

$$I_{abc} = I_{c1} + I_{c2}, \tag{2}$$

$$I_o = I_{c1} - I_{c2}, \tag{3}$$

$$\rightarrow I_{c1} = \frac{I_{abc} + I_o}{2}, \tag{4}$$

$$\rightarrow I_{c1} = \frac{I_{abc} - I_o}{2}, \tag{5}$$

$$V_i = V_{be1} - V_{be2} = V_t[\ln(I_{c1}/I_s) - \ln(I_{c2}/I_s)], \tag{6}$$

$$= V_t[\ln(I_{c1}/I_{c2})], \tag{7}$$

$$= V_t[\ln(\frac{I_{abc} + I_0}{2} / \frac{I_{abc} - I_o}{2})], \tag{8}$$

$$= V_t[\ln(\frac{I_{abc} + I_o}{I_{abc} - I_o})], \tag{9}$$

$$\Rightarrow I_o = I_{abc}[\frac{e^{V_i/V_t} - 1}{e^{V_i/V_t} + 1}]. \tag{10}$$

The first thing to note, is that the OTA gain equation is severely dependent upon V_t. Since $V_t = kT/q$ (where k is Boltzmann's constant, T is temperature, and q is the charge of an electron), the output amplitude will change with temperature. Secondly, as Equations 9 and 10 show, although I_o and I_{abc} are linearly related to each other, neither are linearly related to V_i. This nonlinearity is the major source of distortion in OTAs, and follows an x^3 relationship. This can be seen if we look at the Taylor series expansion (an accurate "approximation") of the natural log in Equation 9:

$$V_i = V_t[\ln(\frac{I_{abc} + I_o}{I_{abc} - I_o})], \tag{11}$$

$$= V_t[\ln(1 + \frac{I_o}{I_{abc}}) - \ln(1 - \frac{I_o}{I_{abc}})], \tag{12}$$

$$\ln(1+x) = x - \frac{x^2}{2} + \frac{x^3}{3} - \frac{x^4}{4} + \frac{x^5}{5} + ..., \tag{13}$$

$$\ln(1-x) = -x - \frac{x^2}{2} - \frac{x^3}{3} - \frac{x^4}{4} - \frac{x^5}{5} + ..., \tag{14}$$

$$\Rightarrow V_i = 2V_t[x + \frac{x^3}{3} + \frac{x^5}{5} + ...] \approx \frac{2V_t I_o}{I_{ac}}, \tag{15}$$

$$\Rightarrow I_o \approx \frac{V_i I_{abc}}{2V_t}. \tag{16}$$

Equation 16 is the usual OTA gain equation shown in the datasheets, and is an approximation. For values of $x \ll 1$, x^3 and x^5 become very small, such that they can usually be ignored. But, this requires that $I_o \ll I_{abc}$, which also means that $V_i \ll V_t \approx$ 26mV. At these low input levels, the OTA noise is a much larger fraction of the signal, and for DC coupled circuits, the offset voltage is on the same order as the signal.

Since I_o is linearly related to I_{abc}, one solution would be to apply the input signal to the control port at I_{abc}. Unfortunately, the input signal must be applied to V_i since it is bipolar. If the control port I_{abc} could accept both positive and negative currents, then it could be used for the signal input and give a far more linear output. As a result of this single sided control port, the OTA is often called a "two quadrant" multiplier. A "four quadrant" multiplier (e.g. LM1496) can be made with two of these OTA sections in parallel, and shows lower distortion when the signal is applied to the control port. Although this fixes the distortion problem, it does not eliminate the temperature dependency.

To eliminate V_t, the Gilbert cell (shown in Figure 4) not only employs a second OTA to work in all four quadrants, but also a third OTA (transistors 3 and 4 in Figure 4) to account for temperature and distortion effects. Since it is the conversion from voltage to current through the input transistors that give rise to both of these problems (see Equation 1), a second set of transistors can be used to perfectly cancel out any nonlinearities. This is done by driving the first stage transistors with a current to create a voltage that drives the second stage transistors, which in turn creates the output current. These first

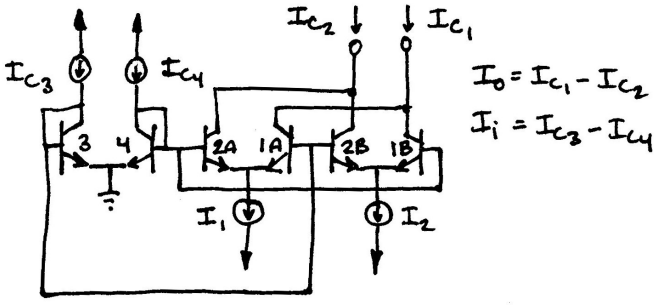

Fig. 4. Gilbert cell multiplier core.

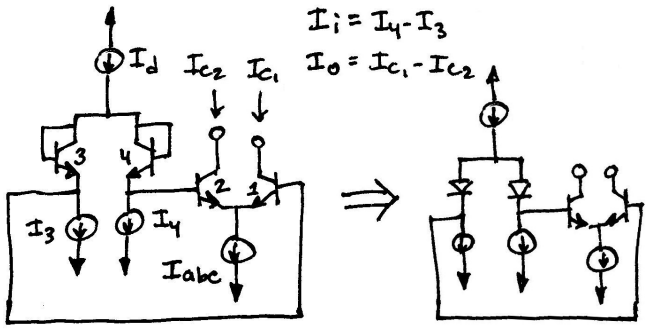

Fig. 5. Linearizing diode configuration in the LM13700.

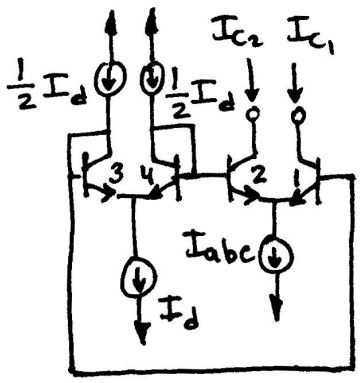

Fig. 6. Linearizing diode configuration in the BA6110 and CA3280.

stage transistors are typically wired as diodes, and are often referred to as "linearizing diodes" or "pre-distortion diodes", as they create an equal and opposite distortion to cancel out the OTA distortion, and linearize the output.

Many OTAs come with linearizing diodes built in. A schematic of their usage in the LM13700 is shown in Figure 5, where the current sources I_3, I_4, and I_d are all externally applied. The output is taken as the difference of the collector currents I_{c1} and I_{c2}, and the input is the difference between I_4 and I_3. If we neglect base currents, we get the following:

$$I_{c4} \approx I_4, \tag{17}$$
$$I_{c3} \approx I_3, \tag{18}$$
$$I_i = I_4 - I_3, \tag{19}$$
$$I_d = I_4 + I_3, \tag{20}$$
$$\rightarrow I_4 = \frac{I_d + I_i}{2}, \tag{21}$$
$$\rightarrow I_3 = \frac{I_d - I_i}{2}, \tag{22}$$
$$V_i = V_{be4} - V_{be3} = V_t[\ln(I_4/I_s) - \ln(I_3/I_s)], \tag{23}$$
$$= V_t[\ln(I_4/I_3)], \tag{24}$$
$$= V_t[\ln(\frac{I_d + I_i}{2} / \frac{I_d - I_i}{2})], \tag{25}$$
$$= V_t[\ln(\frac{I_d + I_i}{I_d - I_i})]. \tag{26}$$

Setting Equation 24 equal to Equation 9 gives:

$$V_i = V_t[\ln(\frac{I_d + I_i}{I_d - I_i})] = V_t[\ln\frac{I_{abc} + I_o}{I_{abc} - I_o}], \tag{27}$$
$$\rightarrow \frac{I_d + I_i}{I_d - I_i} = \frac{I_{abc} + I_o}{I_{abc} - I_o}, \tag{28}$$
$$\Rightarrow I_o = \frac{I_i I_{abc}}{I_d}. \tag{29}$$

This current input to current output OTA relation no longer has a V_t dependency, and is perfectly linear. The I_{abc} term can be thought of as a multiplier, and I_d can be used as a divider. But, all of this depends heavily upon I_d being a fixed current source, and I_i being an accurate difference of I_4 and I_3, which is often not the case. The BA6110 and CA3280 (schematic diagram shown in Figure 6) generate these currents internally, making it much easier to maintain this linear relationship. They also wire the diodes together at the emitters, which improves the accuracy over the LM13700 by changing the way base currents are accounted for. As I_{c3} decreases on the LM13700, I_{c1} increases, increasing the relative proportion of base current which is subtracted from the I_3 signal. In contrast, as I_{c3} decreases on the CA3280, I_{c1} also decreases, keeping the base current error at a fixed ratio.

There are many different ways of driving these diodes, each with their relative merits. And, since the LM13700 comes in a dual package, the second OTA can also be used as the linearizing element. The remaining sections of this paper will analyze each of the different ways this can be done, and discuss their benefits. these methods are:

- Single resistor "current source" compensation
- Single op-amp current source compensation
- Dual op-amp current source compensation
- Dual OTA compensation
- Dual OTA compensation with buffer

Before analyzing the various distortion cancellation schemes, it will be useful to look at the uncompensated circuit to understand its limitations. Although the heart of the OTA is just two transistors, other support circuitry is required to generate the control current I_{abc} and the differential output current I_o. These elements can add significantly to the error of an amplifier.

The control current is generally set with a current mirror, composed of either two or three transistors. I often wished that they left this part off OTAs as the transistors' V_{be} vary with temperature, and therefore cause I_{abc} to vary unless they are driven with an external current source. And even if they are driven with an external current source, the exact current transfer ratio of the current mirror can vary with temperature and current, so there is no guarantee of a fixed operating point. If the mirror was left off entirely, an external current source (which you might be using anyways) could be connected directly to the OTA, giving lower errors. Figure 7 below shows the standard two transistor current mirror employed by the CA3080 and BA662, and Figure 8 shows the three transistor Wilson mirror, which is much better and used by the LM13700, BA6110, and CA3280. Both of these are shown biased with a resistor to set I_{abc}. Figures 9 and 10 show op-

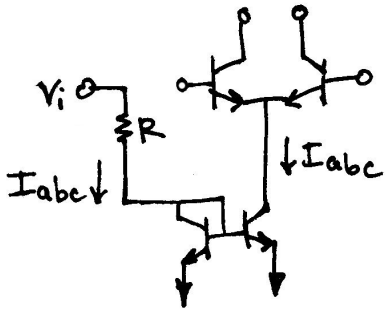

Fig. 7. Two transistor current mirror driving OTA core, with simple resistor biasing.

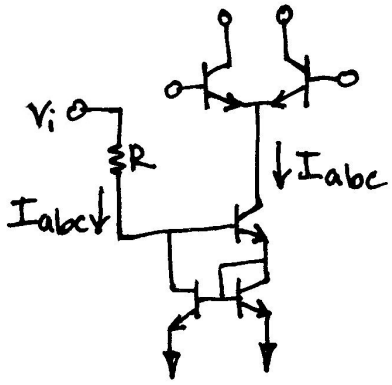

Fig. 8. Wilson current mirror driving OTA core, with simple resistor biasing.

amp current sources, which can be used in conjunction with standard OTAs or with discrete OTAs (custom built).

As can be seen in the simple resistor biasing schemes in Figures 7 and 8, the current flowing into the OTA is a function of both the transistors' V_{be} and the power-supply rails. This means that temperature variations will change the circuit gain, and any noise or drift on the power-supply will be coupled into

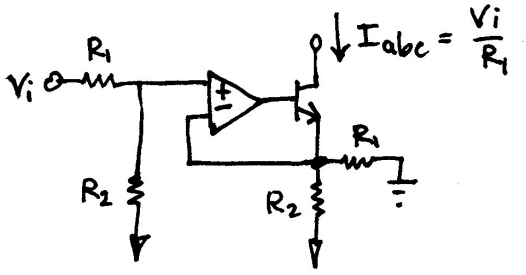

Fig. 9. Non-inverting op-amp current source.

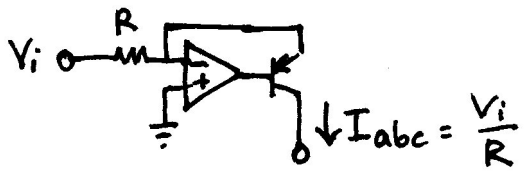

Fig. 10. Inverting op-amp current source.

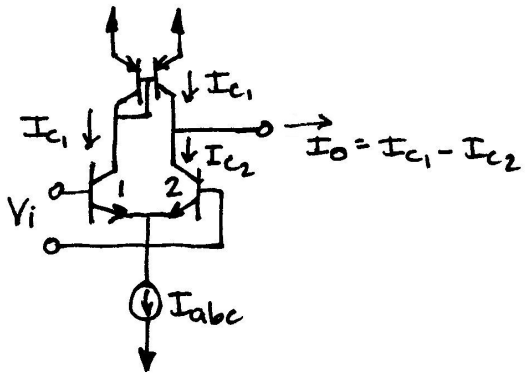

Fig. 11. Single current mirror OTA output stage.

the output. Note the differential nature of the current mirror in Figure 9, which greatly reduces any power-supply effects. The inverting topology of Figure 10 only references ground, avoiding this problem altogether.

Current mirrors are also used to generate the output signal I_o, by inverting one of the differential amplifier signals and adding it with the other. A single mirror example is shown in Figure 11. This topology has the disadvantages of poor output compliance (the output voltage must be larger than the base voltage of transistor 2) and of different V_{ce} values on the transistors of the differential pair. The difference in V_{ce} will create errors in the collector currents due to the Early effect. To eliminate these issues, all commercial OTAs use three Wilson current mirrors, as shown in Figure 2. In this case, one output is inverted once and the other twice, and then both are summed.

To achieve the least distortion from these transistor current mirrors, the output of the OTA should be held at a fixed voltage. This keeps V_{ce} constant on the two output transistors, which minimizes variations in their output resistances and current due to the Early effect. The Darlington buffer transistors supplied with the LM13700 do not do a good job of this. Not only do they have their own V_{be} variations which create errors, but as with any non-inverting buffer configuration, they require the output voltage to vary to create a signal. Using an inverting amplifier (see Figure 12), the output voltage can be kept constant while the output current is converted to a voltage via the feedback resistor.

For discrete OTAs, an op-amp mirror (Figure 13) or a differential amplifier (Figure 14) can be used to calculate the difference in currents. These have the advantage of holding both V_{ce} values the same, and exchanging transistor errors for

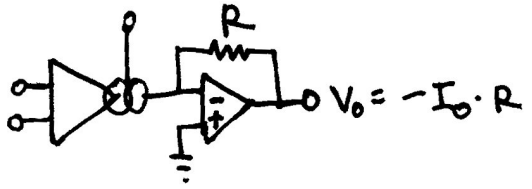

Fig. 12. Inverting op-amp buffer holds OTA output at a fixed voltage.

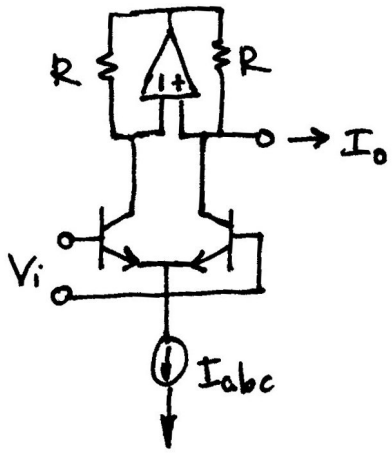

Fig. 13. Op-amp current mirror as output stage of a discrete OTA.

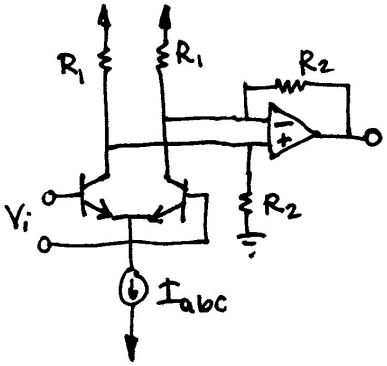

Fig. 14. Op-amp differential amplifier as output stage of a discrete OTA.

resistor errors which can be more carefully controlled. It does add a number of op-amp errors, like input leakage current and offset voltage drift, but these can be limited with the selection of an appropriate op-amp.

Regardless of the output differencing method employed, there will always be slight errors between the input and output currents which lead to output offset voltage issues, distortion, and CV bleed-through (feedthrough). To understand how these arise, we will assume there is a fixed "gain" (a_n) for each current mirror inside the LM13700 and model the differential amplifier core as a perfectly linear multiplier ($I_1 - I_2 = V_i I_{abc} x$). A schematic of this setup is shown in Figure 15, and the output current, I_o, is derived as follows:

$$I_o = I_1 a_1 a_3 - I_2 a_2, \tag{30}$$

$$I_1 - I_2 = V_i I_{abc} x, \tag{31}$$

$$I_1 + I_2 = I_{abc}, \tag{32}$$

$$\rightarrow I_1 = \frac{I_{abc} + V_i I_{abc} x}{2}, \tag{33}$$

$$\rightarrow I_2 = \frac{I_{abc} - V_i I_{abc} x}{2}, \tag{34}$$

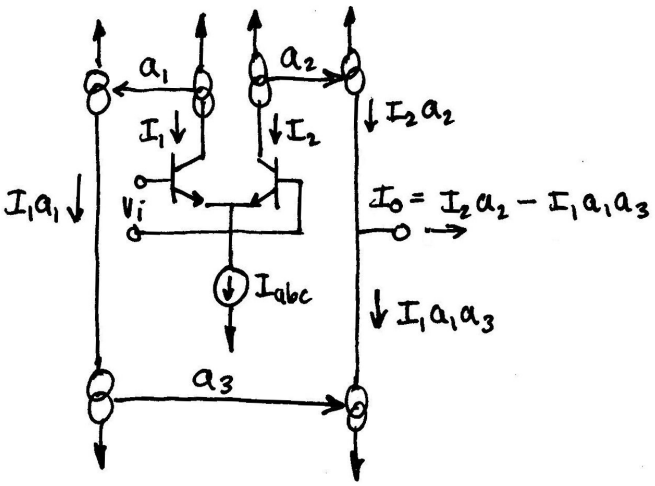

Fig. 15. Error model for OTA output current mirrors.

$$\Rightarrow I_o = (\frac{I_{abc} + V_i I_{abc} x}{2}) a_1 a_3 - (\frac{I_{abc} - V_i I_{abc} x}{2}) a_2, \tag{35}$$

$$= I_{abc}(\frac{a_1 a_3 - a_2}{2}) + V_i I_{abc} x (\frac{a_1 a_3 + a_2}{2}). \tag{36}$$

As can be seen from Equation 36, there are two terms represented in the output signal. One is a linear representation of the input scaled by the current mirror gains, and the second is a replica of I_{abc} scaled by the difference in current mirror gains. So, for conditions where $a_1 a_3 \neq a_2$ there will be a small bit of the control signal at the output, which is known as CV bleed-through. This also gives a fixed offset current at the output for zero input signal.

CV bleed-through can be minimized by adjusting the input voltage slightly, to cancel out the effect. This can be shown if we set our input voltage equal to a signal plus a small offset, and substitute into Equation 36:

$$V_i = V + \Delta V, \tag{37}$$

$$I_o = I_{abc}(\frac{a_1 a_3 - a_2}{2}) + (V + \Delta V) I_{abc} x (\frac{a_1 a_3 + a_2}{2}), \tag{38}$$

$$= I_{abc}(\frac{a_1 a_3 - a_2}{2} + \Delta V x \frac{a_1 a_3 + a_2}{2}) + V I_{abc} x (\frac{a_1 a_3 + a_2}{2}). \tag{39}$$

If the first term in Equation 39 is set to zero, we can solve for a ΔV that eliminates the CV bleed-through. Unfortunately, the differential pair itself has an offset voltage which causes both distortion and an offset current at the output. This offset voltage arises from slight differences between the two input transistors, and slightly shifts the 0V operating point up or down. This turns one transistor on a bit more than the other, creating a slight output current differential. Since the gain of the differential pair is not perfectly linear, this also means that positive input signals will not experience the same gain as negative input signals. One side will distort before the other creating even order harmonics. A perfectly symmetric distortion will only have odd order harmonics.

This leads to a problem where you can eliminate CV bleed-through or even order harmonics, but not both (except in dual

OTA compensation schemes). Ultimately, a trade-off must be made with regard to each, with bleed-through usually being the parameter which is minimized. This could be because bleed-through is more displeasing to hear than even order harmonics, but is more likely due to the ease of trimming it out. This is simply done by applying a CV, setting the input voltage to zero, and trimming until the output current is zero. The feedthrough null point varies with CV level, so it's important to use the average level the circuit will experience, not the maximum. Also, remember to measure across the feedback resistor when using an inverting amplifier as the buffer, and not the output of the buffer, as the former accurately represents the output current whereas the latter includes the buffer's offset voltage. If needed, a second trimmer can be used to compensate for the op-amp's offset voltage. If even harmonics are minimized, a second trimmer is almost always needed to adjust the output offset current of both the OTA and the buffer.

III. Single resistor "current source" compensation

The LM13700 datasheet recommends a simple method of linearizing the response of the amplifier: adding a single resistor. This does reduce distortion, but not always by a large amount. The reason for this, is that the linearizing diodes must be driven with a current source to obtain the theoretical performance shown in Equation 29, and a resistor is not a good substitute for a current source.

In the circuit shown in Figure 16, a resistor is tied to the positive rail, and shorted through the diodes and source resistors to ground. The input source voltage and resistors are combined to their Thevenin equivalents to make analysis easier. To see what effect this method has on the output, we can examine the current through R_d and see how well it approximates a current source. A schematic representation of the input circuitry is shown in Figure 17, with base currents neglected.

The exact transfer function of the input stage can not be reduced to a closed-form solution, as it contains a transcendental function. But, a great deal of insight can be gained from looking at the general form and using approximations. The input voltage is applied as a difference between V_3 and V_4, and this creates a change in V_i which drives the differential amplifier stage. This gives the following relations:

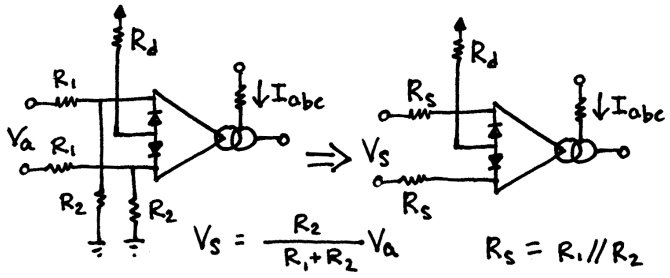

Fig. 16. Example of differentially driven, single resistor compensation and its Thevenin equivalent circuit.

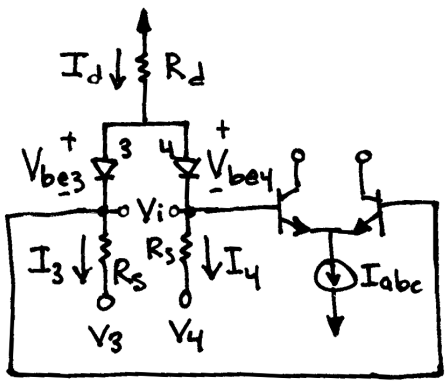

Fig. 17. Input model of differentially driven, single resistor compensation circuit.

$$I_3 = \frac{V_d - V_{be3} - V_3}{R_s} = I_s e^{V_{be3}/V_t}, \tag{40}$$

$$I_4 = \frac{V_d - V_{be4} - V_4}{R_s} = I_s e^{V_{be4}/V_t}, \tag{41}$$

$$I_d = \frac{V_{cc} - V_d}{R_d}, \tag{42}$$

$$\rightarrow V_d = V_{cc} - I_d R_d, \tag{43}$$

$$I_d = I_3 + I_4, \tag{44}$$

$$= \frac{V_d - V_{be3} - V_3}{R_s} + \frac{V_d - V_{be4} - V_4}{R_s}, \tag{45}$$

$$= \frac{2V_d - V_{be3} - V_{be4} - V_3 - V_4}{R_s}, \tag{46}$$

$$= \frac{2(V_{cc} - I_d R_d) - (V_{be3} + V_{be4}) - (V_3 + V_4))}{R_s}, \tag{47}$$

$$\rightarrow I_d = \frac{2V_{cc} - \Sigma V_{be3,4} - \Sigma V_{3,4}}{R_s + 2R_d}. \tag{48}$$

The first thing Equation 48 shows, is that the current through the diodes is temperature dependent, as it is a function of V_{be3} and V_{be4}. The only way to reduce this effect is to operate at $V_{cc} - \Sigma V_{3,4} \gg \Sigma V_{be3,4}$. Ultimately, this is a bit difficult to accomplish, as $V_{cc} - \Sigma V_{3,4}$ is limited by the power-supply ($\pm$15V = 30V) and $\Sigma V_{be3,4}$ $\approx$1.2V. So there will always be an $\sim$4% temperature dependent component to I_d.

The second thing to note is that I_d is also a function of the sum of the input voltages V_3 and V_4. Luckily, this error term can be eliminated by applying a differential input voltage ($V_3 = -V_4$). In this way, as V_3 increases, V_4 decreases by that exact same amount, keeping $\Sigma V_{3,4}$ constant.

Finally, as the input signals change so do V_{be3} and V_{be4}, resulting in a net change in I_d. If we use a differential input, this becomes the only error term (ignoring temperature effects). So exactly how large is the change in $\Sigma V_{be3,4}$ with an input signal? This is a function of the magnitude of the input signal, and can be approximated as follows (assuming $\Delta I = I_3 - I_4$ and $\Delta I_d / I_d \ll 1$):

$$I_{3_0} = I_{4_0} = \frac{I_d}{2}, \quad (49)$$

$$I_{3_1} = \frac{I_d}{2} + \frac{\Delta I}{2}, \quad (50)$$

$$I_{4_1} = \frac{I_2}{2} - \frac{\Delta I}{2}, \quad (51)$$

$$\Sigma V_{be3,4} = V_t \ln(\frac{I_3}{I_s}) + V_t \ln(\frac{I_4}{I_s}) = V_t \ln(\frac{I_3 I_4}{I_s^2}), \quad (52)$$

$$\Sigma V_{be3,4_0} - \Sigma V_{be3,4_1} = V_t \ln(\frac{I_{3_0} I_{4_0}}{I_s^2}) - V_t \ln(\frac{I_{3_1} I_{4_1}}{I_s^2}), \quad (53)$$

$$= V_t \ln(\frac{I_{3_0} I_{4_0}}{I_{3_1} I_{4_1}}), \quad (54)$$

$$= V_t \ln(\frac{\frac{I_d}{2}\frac{I_d}{2}}{(\frac{I_d}{2} + \frac{\Delta I}{2})(\frac{I_d}{2} - \frac{\Delta I}{2})}), \quad (55)$$

$$= V_t \ln(\frac{1}{(1 + \frac{\Delta I}{I_d})(1 - \frac{\Delta I}{I_d})}), \quad (56)$$

$$= -V_t \ln((1 + \frac{\Delta I}{I_d})(1 - \frac{\Delta I}{I_d})). \quad (57)$$

The maximum input signal (ΔI) has to be less than I_d, as this is the total current supplied to the input circuitry. At an input of 90% full scale this gives a change in $\Sigma V_{be3,4}$ of only 43mV. This is a relatively small error, so if a differential input signal is used, a single resistor linearizing scheme can work quite well. But, this is only one half of the requirement for low distortion, the other half is the need to have the input signal linearly produce a current difference between the two diodes. Using Equations 40, 41, 50, and 51, this can be derived as follows:

$$\Delta I = I_3 - I_4, \quad (58)$$

$$= \frac{V_d - V_{be3} - V_3}{R_s} - \frac{V_d - V_{be4} - V_4}{R_s}, \quad (59)$$

$$= \frac{\Delta V_{be3,4} + \Delta V_{3,4}}{R_s}, \quad (60)$$

$$= \frac{V_t \ln(I_4/I_3) + \Delta V_{3,4}}{R_s}, \quad (61)$$

$$= \frac{V_t \ln((1 - \frac{\Delta I}{I_d})/(1 + \frac{\Delta I}{I_d})) + \Delta V_{3,4}}{R_s}. \quad (62)$$

Since $\Delta V_{3,4}$ is the input signal, it is almost a perfectly linear relationship, except for V_{be} effects. As with keeping I_d linear, we gain an advantage by using large voltages, this time at the input signal. If we assume $\Delta V_{be3,4}$ is small, and use the maximal $\Delta I = I_d$, then $\Delta V_{3,4} \approx I_d R_s$. This value is constrained to be below the power-supply rails as ΔI flows through R_s, so 15V would be a reasonable maximum to assume. $\Delta V_{be3,4}$ for a 90% full scale input swing is then only 76mV, which is much smaller than 15V, giving relatively low distortion. But, there is still a temperature dependency.

Ultimately, using only resistors is an inexpensive and compact design with decent performance, if implemented correctly. Unfortunately, the example schematics in the LM13700 datasheet (shown in Figure 18) are not optimal implementations. They show an R_s of 500Ω and an R_d of 13kΩ, which

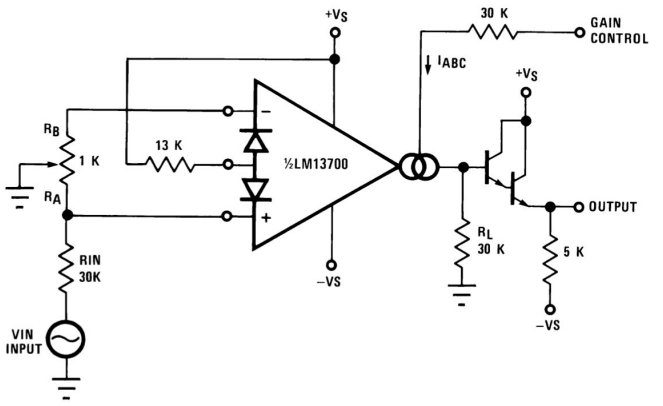

Fig. 18. Example of LM13700 with single resistor compensation from TI datasheet.

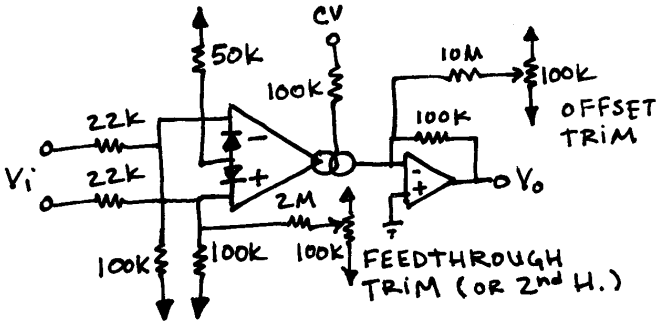

Fig. 19. Example of single resistor compensation with differential input, offset trimmers, and maximized source resistance.

gives an I_d of approximately 1mA. This large value for I_d causes errors due to non-negligible base currents and bulk emitter resistance drops. From my experience, i have found a value of 250μA to be a better upper limit. Another problem is the offset trimming solution, which causes an imbalance in R_s and has too large of a trimming range. A better solution is shown in Figure 19.

The largest source of error in the TI example is the single ended input, and this is a more complicated issue. If a differential signal exists from a previous stage, then it can be easily applied to the inputs. But, for other cases an inverting op-amp must be used to create the differential source (as shown in Figure 20), which greatly reduces the simplicity of the circuit. And, if an op-amp is to be added, it can be used as a true current source, as detailed in next section.

A number of differential solutions are shown in Figures 16, 19, and 20. The objective with all of these is to maximize the values of R_d and R_s so that the input signals more closely mimic current sources (current sources are high impedance, whereas voltage sources are low impedance). To accomplish this, larger voltages are required. For this reason, Figures 19 and 20 show the source resistors tied to the negative supply voltage. For Figures 16 and 19, the output impedances of both drivers must be matched, or very small.

For single ended inputs, maximizing R_s is not the best solution. The reason for this can be seen in Equation 48, which shows that I_d is a strong function of $\Sigma V_{3,4}$. Since

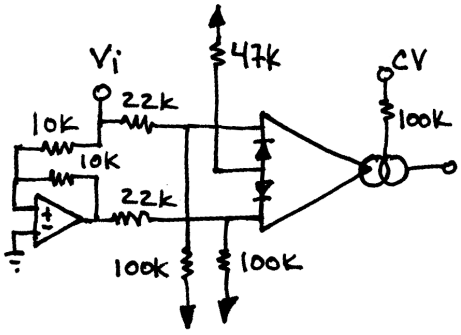

Fig. 20. Example of single resistor compensation, differentially driven with an op-amp and using the negative supply to increase R_s.

$\Sigma V_{3,4} = \Delta V_{3,4}$ for a single ended source ($V_4 = 0$), by reducing R_s we reduce the $\Delta V_{3,4}$ required to obtain the same input signal ($\Delta I \approx \Delta V_{3,4}/R_s$). This works well up to the point where $\Delta V_{3,4}$ is on the same order as $\Delta V_{be3,4}$, such that ΔI is no longer linearly related to the input signal (see Equation 60). So a compromise must be made between the asymmetric (even harmonic) distortion that arises from large R_s values and I_d variations, and the symmetric distortion of small R_s values and ΔI nonlinearities.

This trade-off is shown in Figures 21–23, where the distortion levels are given for varying R_s values and input signal levels. In Figure 21, the second harmonic levels rise for increasing resistance, and in Figure 22 the third harmonic levels decrease for increasing resistance. It is important to note that it is the ratio of R_d/R_s that is relevant, so for smaller values of R_d, smaller values of R_s must be used to obtain the same level of distortion. Figure 23 shows the total distortion versus resistance, which has minimums from 500Ω to 2kΩ. This gives $R_d/R_s \approx 25$ to 100 for the 47kΩ R_d used in these experiments. It can now be seen why the TI datasheet recommends an R_s of 500Ω, as this gives an R_d/R_s ratio of 13kΩ / 500Ω = 26, which falls within this range.

The best R_d/R_s ratio to use is application dependent. Is second or third harmonic distortion more problematic? What is the maximum input amplitude? Will the circuit be trimmed

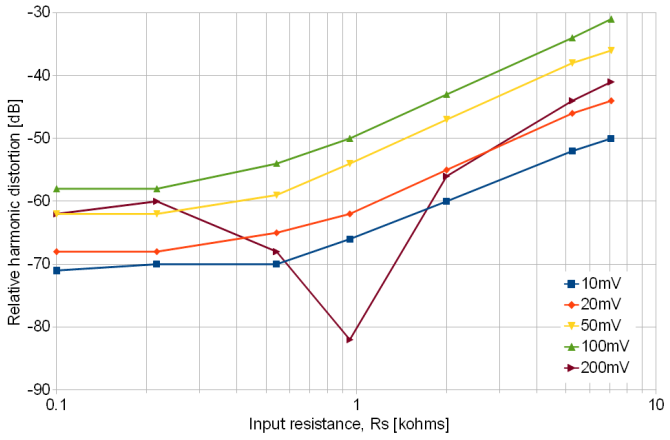

Fig. 21. 2^{nd} harmonic distortion versus input source impedance (R_d = 47kΩ) for varying input levels. Single ended input with feedthrough nulled.

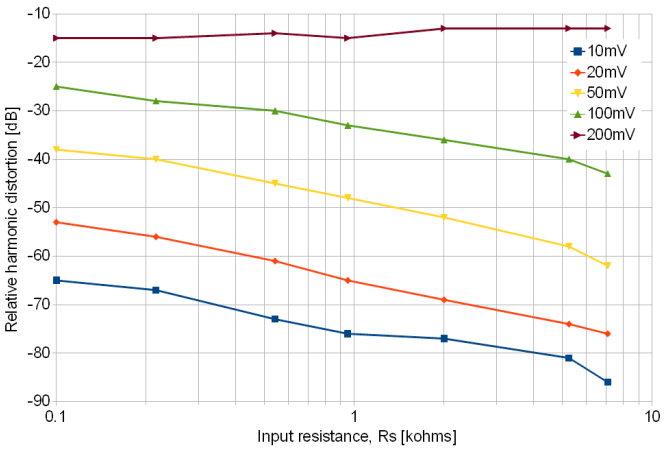

Fig. 22. 3^{rd} harmonic distortion versus input source impedance (R_d = 47kΩ) for varying input levels. Single ended input with feedthrough nulled.

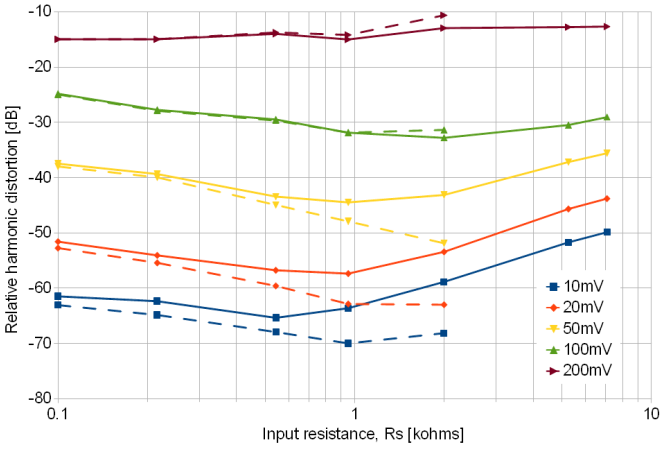

Fig. 23. Linear sum of 2^{nd} and 3^{rd} harmonic distortion components versus input source impedance (R_d = 47kΩ) for varying input levels. Single ended input with dashed line showing 2^{nd} harmonic null trimming, and solid line showing feedthrough null trimming.

for CV bleed-through or second harmonic distortion? Does temperature drift need to be minimized? The temperature compensating effects of the linearizing diodes are increased for larger values of R_s. Also, the second harmonic can not be nulled for large values of R_s (which is why the curves stop at 2kΩ in Figure 23). Above this point, the I_d variation induced distortion is too great to overcome. For most applications, the inherent second harmonics are larger than the third harmonics, making slightly smaller R_s values preferable, as this helps reduce the larger of the two distortions. An R_d/R_s value of 50 is a good compromise given these concerns.

IV. Single Op-Amp Current Source Compensation

In order to achieve the ideal temperature compensation and linearization effects of the pre-distortion diodes, the input signal needs to linearly change the current between them, and I_d must be kept constant. With a single op-amp you can only do one of these tasks well (without adding other devices such as transistors or current mirrors). The question then becomes, which parameter should be controlled by the external op-amp?

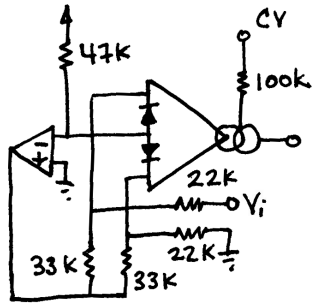

Fig. 24. Example of single op-amp constant current source driving linearizing diodes.

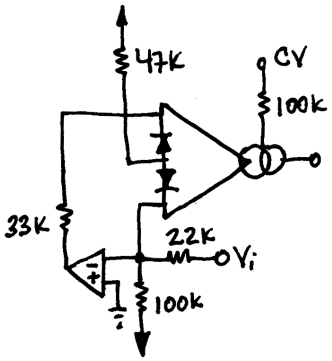

Fig. 25. Example of single op-amp differential current source driving linearizing diodes.

As it turns out, the answer to this question is both a function of theoretical performance and practical circuit design. Figure 24 shows one possible solution to keeping I_d constant, and Figure 25 shows an alternate which fixes ΔI_d to be proportional to the input signal. They both give similar performance, but Figure 25 is very sensitive to the power-supply voltage and would quickly drift out of calibration. The reason for this, is that the circuit holds the current through one diode fixed, but the total current through both diodes will fluctuate with V_{be} and V_{cc}. This leads to an imbalance for the no-signal condition.

Holding I_d constant is a better approach to minimizing temperature drifts. From Equation 48, it can be seen that the I_d error is related to $\Sigma V_{be3,4}$, whereas from Equation 60 the error in ΔI_d is related to $\Delta V_{be3,4}$. Since $\Delta V_{be3,4}$ will always be smaller than $\Sigma V_{be3,4}$, the temperature drift in ΔI_d will always be smaller than in I_d. Furthermore, $\Delta V_{be3,4}$ does not have an I_s term in it, making it more stable than $\Sigma V_{be3,4}$. Since I_s is far more volatile than V_t, it is better to hold I_d constant.

This approach of holding I_d constant is employed in the CA3280 and the BA6110 by using current mirrors to drive the linearizing diodes (see Figure 26). The distortion performance of these OTAs is identical to an LM13700 implemented as shown in Figure 24. But, because they use current mirrors on both sides of the diodes, the circuit in Figure 25 can actually be used to improve their performance (sans the 100kΩ pull-down resistor). The reason for this, is that I_d is already being held constant, and Figure 25 linearizes ΔI_d, making it theoretically

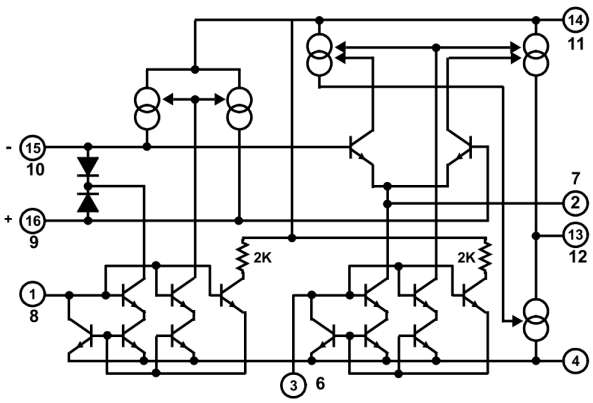

Fig. 26. Internal wiring diagram of CA3280 showing linearizing diodes driven by current sources (from Intersil datasheet).

ideal. The temperature drift issues are also eliminated due to the individual diode currents being set to exactly one half by another set of current mirrors.

V. Dual op-amp current source compensation

To overcome the short-comings of the single op-amp method, a second op-amp can be employed to fix both I_d and ΔI_d (see Figures 37 and 38). Or, similar to the CA3280, current mirrors can be used in place of the op-amps. These topologies show improvement over the single op-amp methods, but add a great deal of complexity.

The main reason for this added complexity, is that transistors must be employed to accomplish at least one of the tasks. The standard method of fixing a current with an op-amp involves setting a fixed voltage at its non-inverting terminal, connecting a resistor to its inverting terminal, and forcing the current through that resistor into the node under current control. The problem with this method is that it holds the driven node at a fixed voltage, and only one side of the diodes can be held at a fixed voltage, the other side must be free to change voltage with applied signal. Therefore a current source with voltage compliance is required, which can be accomplished by adding a transistor. Ultimately, all of these extra parts add extra

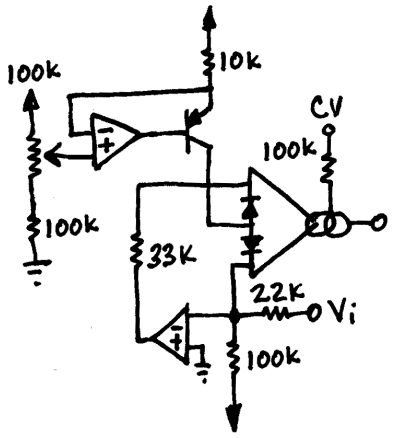

Fig. 27. Dual op-amp compensation with I_d driven with a transistor.

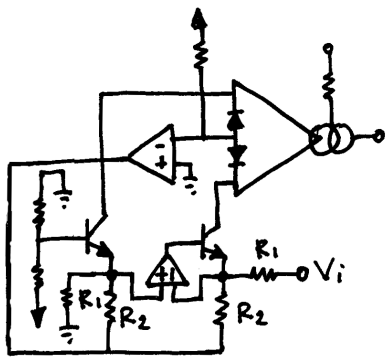

Fig. 28. Dual op-amp compensation with ΔI driven by transistors.

sources of noise and error, making the dual op-amp schemes undesirable.

VI. Dual OTA compensation

All of the above distortion minimizing techniques rely on the linearizing diodes accurately compensating for the nonlinearities of the input differential pair. Unfortunately, this diode approximation is not completely accurate, and has an error of at least $1/\beta$ (where β is the transistor current transfer ratio). An ideal compensation method would have an identically matched differential pair being driven in the same manner. Luckily for us, the LM13700 is a dual OTA and has exactly that. This idea was detailed by Mike Sims in 1995 (http://www.teaser.fr/~amajorel/sims/).

As shown in Figure 29, the first OTA is being driven with a fixed I_{abc}, and its output is held equal to the input signal via negative feedback around the OTA. This feedback creates a distorted drive signal (ΔV_{be}) for the first OTA which forces the output to generate a perfectly linear replica of the input signal. In this manner, the output distortion is eliminated on the first OTA. And, since the first and second OTAs share the same ΔV_{be} and are well matched, they produce the same output: a linear replica of the input signal.

Although this circuit works well in practice, it still has a nonlinearity. Since the feedback around the first OTA must generate a finite ΔV_{be} to create an output signal, and since the positive terminal is fixed at ground, the summing junction at the negative terminal becomes non-zero for any non-zero input signal. This means that the current flowing through the input resistor, which becomes the output current, is no longer an accurate replica of desired input signal. The actual relationship is:

$$\frac{V_i - \Delta V_{be}}{R} = -I_o + I_{b1} + I_{b2}, \tag{63}$$

where I_{b1} and I_{b2} are the input bias currents into the OTAs. Since ΔV_{be} is fixed for a given output current, making V_i as large as possible will minimize this error. But, there is also the bias current error, which is on the order of I_{abc}/β and fluctuates with I_o.

Since the first OTA requires a compensation capacitor for stability (the 330pF capacitor in Figure 29), at high frequencies some of the current will go into the capacitor. This creates another error term, where the output current no longer accurately reflects the input signal. This can be fixed with an op-amp, which will be described in the next section.

Using a second OTA for the distortion compensation has a secondary advantage over the linearizing diodes, and this arises from the fact that the two OTAs are not hard wired to have an identical ΔV_{be}, as is the case with the linearizing diodes. This means that both offset voltage in the input differential pair, and offset current in the internal current mirrors of the OTA can be trimmed independently. With single OTA methods, either one or the other error can be eliminated, but not both. With dual OTA methods, both CV bleed-through and second harmonic distortion can be minimized.

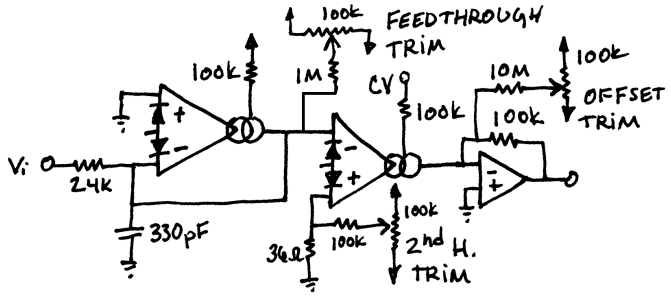

Fig. 29. Dual OTA compensation schematic.

VII. Dual OTA compensation with buffer

To eliminate the input current errors on the dual OTA scheme, a buffer op-amp can be employed to drive ΔV_{be}. This makes the output of the first OTA a perfect replica of the input signal. A schematic of this configuration is shown in Figure 30. The compensation capacitor error can also be eliminated in this scheme, by feeding an inverted version of the error signal into the final output stage. For this reason, the two 1nF capacitors in Figure 30 must be closely matched, and the drive signal must be applied to the non-inverting input on the second OTA.

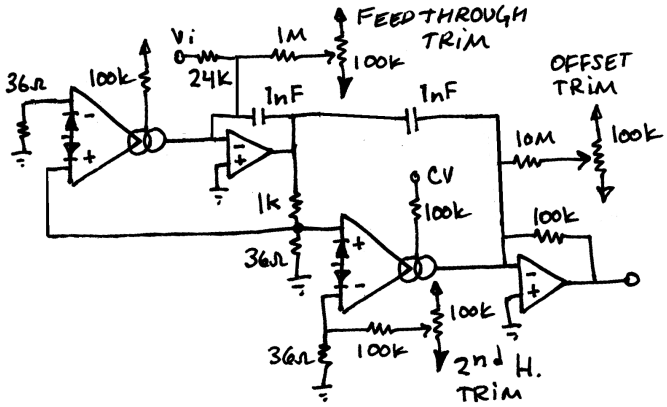

Fig. 30. Dual OTA compensation with buffer and trimming.

VIII. Results

The various compensation techniques were built and tested, all using the same LM13700 OTA and OP297 op-amp, to eliminate part variations. They were also designed to have the same gain, with a 1Vpp input signal generating a 4Vpp output signal (with a 100kΩ feedback resistor around the output buffer). Since they had identical I_{abc} and I_d values (both ∼230μA), they also had very similar input impedances. The circuit inputs were stepped through 1V, 2V, 5V, 10V, and 20V, generating 10mVpp to ∼200mVpp ΔV_{be} at the OTA inputs, respectively. For each of these input levels, the output feedback resistor was scaled to give a 1Vrms output, to keep any amplitude induced distortions to a minimum. The second and third harmonic levels were then recorded, but the 200mVpp levels are not shown as these were deep into the saturation region of the OTA. The noise floor and CV bleed-through were also measured for a grounded input using a 100kΩ output resistor.

The second and third harmonic distortion for these topologies are shown in Figures 31 and 32, respectively. The uncompensated scheme is included for reference. These were all conducted with feedthrough trimmed out, as this is the more likely use scenario, although it does not reflect the best theoretical performance. The exceptions to this are the dual OTA schemes, which can be trimmed for both feedthrough and second harmonic, and these results are shown in dashed lines. No dashed lines appear in Figure 32 as the level of trimming (either second harmonic or feedthrough) does not effect the third harmonic. All topologies can be trimmed for second harmonic null to varying degrees, but this causes severe degradation of feedthrough performance. For the OTA tested here, feedthrough was +50dB worse with the second harmonic nulled (except on dual OTA schemes which are turkeys with all the trimmings).

The schematics for the circuits used can be found in the previous sections of this document. Most are shown exactly as built, except for the single resistor and uncompensated versions (Figure 16 with one input tied to ground). The single resistor version used R_d = 47kΩ and R_s = 1kΩ (comprised of a 1kΩ resistor to ground and a 19.5kΩ resistor to the input signal). The uncompensated scheme did not have an R_d, and used a 100Ω resistor to ground and 6.8kΩ resistor to the input signal. The differentially driven single resistor version is shown in Figure 20. The single and dual op-amp schemes tested are the constant I_d versions shown in Figures 24 and 27, respectively.

The single resistor compensation scheme performs quite poorly, unless differentially driven, in which case it performs surprisingly well. In single sided mode, the second harmonic distortion is actually worse than the uncompensated scheme, and the third harmonic is only -10dB better. This is to be expected, as lower resistances give better even harmonic performance, and the uncompensated scheme has a source resistance of 100Ω. But, as detailed in Section III, the total distortion is better for slightly higher resistances.

The differential, single resistor method has -15dB better second harmonic performance and -25dB better third harmonic

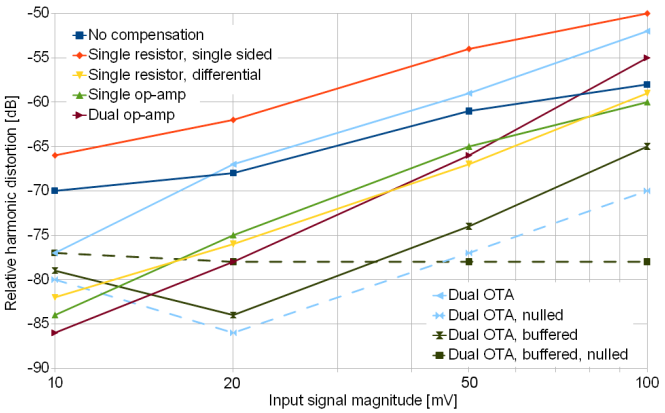

Fig. 31. Second harmonic distortion versus input signal level (ΔV_{be} peak to peak value) for tested topologies. Solid lines are feedthrough nulled, dashed lines are both feedthrough and second harmonic nulled.

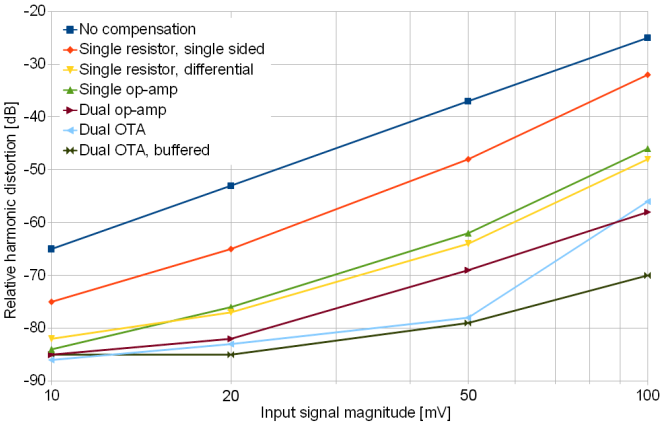

Fig. 32. Third harmonic distortion versus input signal level (ΔV_{be} peak to peak value) for tested topologies, feedthrough nulled.

performance in comparison to the uncompensated scheme. This is actually slightly better than the single op-amp method (although temperature drift would be slightly worse). The reason for this, is that the single op-amp method holds I_d constant, eliminating its $\Sigma V_{be3,4}$ distortion components, but still has $\Delta V_{be3,4}$ errors. With the differential, single resistor method, I_d is allowed to vary a bit, reducing $\Delta V_{be3,4}$ at the expense of increasing $\Sigma V_{be3,4}$. The net sum of these two components is less than in the single op-amp version, as $\Sigma V_{be3,4}$ is dwarfed by $2V_{cc}$ in Equation 48. Differentially driving the single op-amp method shows no improvement in its distortion levels.

Unique to these two topologies, is that increasing the input resistance will improve performance (as detailed in Section III). But, the only way to do this is to reduce I_d, as R_s is proportional to $1/I_d$. From tests with reduced I_d (54μA down from 230μA), distortion dropped by 6dB for the single op-amp version, and by 10dB for the differential, single resistor version. Again, since $\Delta V_{be3,4}$ is fixed for a given output swing, minimal gains can be had by increasing R_s for the single op-amp version.

The dual op-amp scheme also performed very well, with similar second harmonic distortion to the single op-amp

version, but with approximately 10dB better third harmonic distortion. Ultimately, these levels could be achieved with the differential, single resistor method, so it's not clear that the added complexity and cost of this circuit is warranted. The power-supply dependencies and their associated drifts also reduce the practicality of this circuit.

The unbuffered dual OTA scheme has horrendous second harmonic distortion, which is worse than an uncompensated amplifier. This arises due to the ΔV_{be} component of the input signal, along with the high frequency phase shift due to the compensation capacitor. These effects can be trimmed out to a certain degree, but it's unclear how this trimming drifts over time and various I_{abc} drive levels. This makes an inherently lower distortion topology more favorable. But, the third harmonic levels are very good, almost the same as the buffered dual OTA scheme.

There are some limitations to the accuracy of the results presented. The circuits were driven with an HP-33120A signal generator, and the output harmonics and noise floor were measured with an HP-3561A dynamic signal analyzer. The signal generator has a limited noise floor, and -75dB second harmonics. This is fine for most of the measurements which were much higher than this, but for the dual OTA schemes second harmonic trimming was difficult. It became unclear whether the distortion level was a result of the circuit or the signal generator. This is further compounded by the fact that higher distortion at higher drive levels can be trimmed out and "shifted" down to the lower levels, averaging out the total distortion. An example of this can be seen in the dual OTA results in Figure 31. The distortion ramps back up again below the 20mVpp level, after falling at the exact same slope as the uncompensated results. It can be seen that this is just a shift of the already present distortion. For the buffered version, the distortion level bottoms out at -77dB, and is constant across the whole range, which suggests that the actual circuit induced distortion is much lower, as this is merely the signal generator's contribution.

Further compounding these uncertainties is the limited noise floor of the dynamic signal analyzer. The analyzer can dynamically adjust to varying signal levels, but only has an 85dB SNR at any particular level. This means that signals below -85dB can not be measured if a 0dB signal is present, which was the case for all of the distortion measurements. So, for the low input signal cases, the third harmonic distortion is most likely much lower for dual OTA schemes. For feedthrough and SNR measurements, the limited dynamic range is not a problem, as a 0dB signal does not exist and the analyzer can scale the input appropriately.

CV bleed-through was tested with a 20Vpp signal driving the I_{abc} input through a 100kΩ resistor. The output for the majority of topologies showed a signal with equal first and second harmonics of around -68dB. This is referenced to a 1Vpp circuit input. Comparing to a 10Vpp input (maximum level before clipping) would give -88dB bleed-through. The dual op-amp and dual OTA schemes performed slightly worse than the other circuits, by around +5dB. It's uncertain whether this is due to inherent offsets in the circuits, or the fact that they have more parts with high impedance nodes, leading to stray capacitance pick-up of the very large 20Vpp signal nearby. For the unbuffered dual OTA scheme, feedthrough was markedly better when the second OTA was driven at its inverting input (as show in Figure 29) as compared to its non-inverting input. But, the output noise is worse in this configuration. Again, it's unclear why this is the case, but is most likely due to circuit layout and coupling effects.

The output noise of the various topologies followed similarly to the feedthrough results. Most topologies have 72dB SNR compared to a 1Vpp input signal. This becomes 92dB when compared to the maximum input of 10Vpp, which is very similar to the noise level shown in the LM13700 datasheet. Again, the dual op-amp, unbuffered dual OTA, and buffered dual OTA schemes performed worse, with noise being +3dB, +6dB, and +10dB above the others, respectively. The dual OTA schemes are much more sensitive to pick-up and power-supply noise and have the noise of the first stage being amplified by the second. So, it's not surprising to see a +6dB increase. But, if the ability to run at higher signal levels to achieve better SNR is the goal, the +10dB noise floor increase begins to counteract the distortion benefits.

IX. Conclusions

The OTA is a very useful circuit element that can be easily improved with a few more components. The relative benefits of single resistor compensation are minimal, but so is the added cost of a single resistor, making it worthwhile if total distortion is of primary concern. If even harmonic distortion is the limiting factor, then the uncompensated amplifier is preferred. The temperature compensating effects of this topology are also minimal. Both uncompensated and single resistor methods feature a gradual decline into distortion and clipping, whereas the more accurate topologies go straight into heavy clipping during overload conditions.

For most applications, the addition of a single op-amp can give great gains, whether used as a differential driver or as a constant I_d driver. The differential, single resistor topology is slightly better, but also slightly more prone to gain drift, both due to temperature and power-supply variations. With a good reference voltage, I_d will be held very constant in the single op-amp topology, whereas the differential, single resistor topology would require both positive and negative reference voltages and would still drift due to V_{be} variations. Also, offset voltage drifts in the op-amp will imbalance the null trimming for the single resistor version. But, these are relatively minor issues, and both circuits are good options, with performance identical to the CA3280 or BA6110.

The dual op-amp topology gives slightly better distortion results, but is probably not worth the extra complexity, cost, noise, and feedthrough. But, there may be a more elegant circuit implementation that fixes some of these problems. For designs that are already using matched pairs, dedicated current mirrors could be built to replicate a lot of this topology's functionality. The constant I_d variant tested here has severe power-supply dependencies, which could be reduced with a dedicated reference voltage.

The dual OTA schemes are very appealing, but they require a great level of detail for their implementation. They are

extremely sensitive to power-supply and pick-up noise, so compact and well routed designs with closely decoupled supplies are required. This is not very costly in terms of part count, but very costly in terms of design and testing. The extra noise and bleed-through are concerning, but these can probably be fixed with good layout and perhaps reduction of the compensating op-amp's gain. Ultimately, if that level of detail is going to be implemented, the buffered dual OTA scheme is the better option, as it's just one more op-amp for a lot of improvement. The ability to trim both second harmonic and feedthrough is a great benefit of these schemes, but relying on second harmonic trim to fix the errors in the unbuffered version is risky, as it requires a large trim, and offset drifts could easily push the circuit back to its normally awful performance.

Ultimately, the LM13700 is an inexpensive part that can made into a decent multiplier. These schemes improve both distortion and temperature stability for very little cost (2$US). They also produce a signal at the input that is "pre-distorted", and if used as an output, has a unique distortion characteristic which is different from common soft clipping distortion. For precision multiplication, the AD633 by Analog Devices is a good choice, although for a much larger cost (10$US). But, a careful comparison would need to be made between the two

X. Addendum – October 24, 2018

A. Stability of dual OTA compensation with buffer

Although the buffered, dual OTA performed very well from a distortion perspective, the circuit built in the original work was highly unstable. It suffered from both internal noise, and pickup noise. The reasons for these alluded me at the time, so i went back to understand them better. The result is the schematic shown in Figure 33, with much improved stability and noise performance.

The main problem with the original design (Figure 30), was the feed-forward capacitor between the output of the first stage op-amp to the input of the second stage op-amp. This created a differentiator that amplified any high frequency signals at the output of the first stage. What is worse, is that the gain of this amplification increased indefinitely with frequency, as the gain of the second stage inverting op-amp is $100\text{k}\Omega \times 100\text{nF} \times 2\pi f$, where f is the frequency of interest. This greatly increased the amount of high frequency noise from the OTA, and the circuit's response to pick-up and power-supply noise.

The reason this capacitor was used, was to cancel out the phasing effects of the feedback capacitor in the first stage, which was required for stability. But, by using a different stability compensation technique (as is used on the SSM2164, CEM3340, etc.), both capacitors could be eliminated. As a result, the circuit became much more stable, and noise was greatly reduced. The noise is still higher than for single OTA schemes, as there are 2 OTAs adding up their individual noise components, but this is in the range of +3dB to +6dB as compared to the original +10dB.

The new stability components are the resistor and capacitor labeled R and C, respectively, in Figure 33. These reduce the impedance seen at the input of the first stage op-amp at higher frequencies, reducing the gain of the feedback loop. This also reduces the noise picked up at this usually high impedance node. For the circuit tested, a TL082 op-amp was used, and R = 2kΩ and C = 50pF were required to reduce the gain enough to stop oscillation. These should be taken as minimum values which will vary with the op-amp used, temperature, and other variables. Values ranging down to 560Ω and up to 1nF were tried, and showed no difference in frequency response or noise in the audible range. So more conservative values than the minimum are recommended.

B. Alternate current source for constant I_d

The most cost effective method of improving the distortion of an OTA was to add a single op-amp as a constant current source for the diode current. This improved the LM13700 performance to that of a CA3280 for around 0.20$US at medium quantities. An alternate method of accomplishing this using a spare half of an LM13700 is shown in Figure 34. Here, the spare OTA is used as a constant current source which directly supplies the linearizing diodes.

This has the advantage over the other dual OTA schemes in that it less expensive, more stable, and lower noise, although not as low distortion as the buffered dual OTA. It also is less expensive than the single op-amp schemes (assuming an unused LM13700 half), but is slightly less temperature stable as the current source is dependent upon the V_{be} of the I_{abc} input and the linearizing diodes. The former can be rather

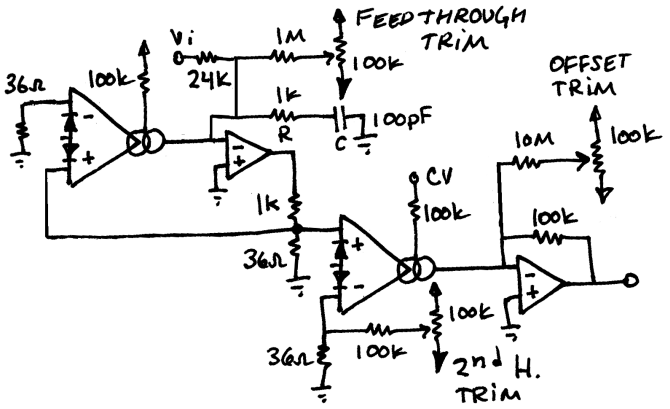

Fig. 33. Improved dual OTA compensation scheme with buffer.

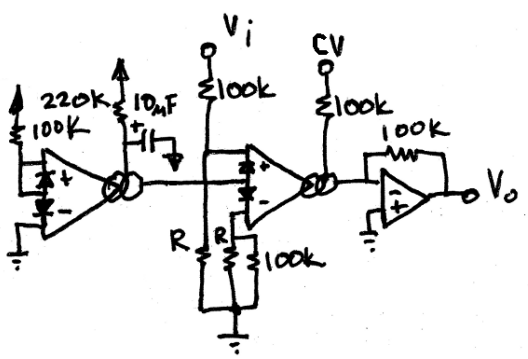

Fig. 34. Alternate I_d employing one half of an LM13700.

small as the voltage drop across the I_{abc} setting resistor is quite large (22V or more for $\pm$12V rails) compared to possible V_{be} variations. The latter is negligible as the OTA is held in saturation. A 10μF capacitor can be placed between the I_{abc} input and $-V_{cc}$ to reduce power-supply and pickup noise.

C. Optimal input resistance for constant I_d schemes

In Section III of the original work, the distortion versus input resistance was analyzed, as this played a large role in the trade-off between keeping I_d "constant" with a single resistor, and mimicking a differential current source with the input signal. But, for the single op-amp scheme presented in Section IV, it was assumed that larger resistors would be better, as I_d was already being held constant, so mimicking a differential current source at the input was the only priority. But, this turns out to not be the case, as second harmonic distortion increases with increasing resistance, just as in the single resistor schemes.

There is a finite offset current at the input of the OTA due to imbalances in β of the input differential pair transistors. This current flows through the input resistors and linearizing diodes, causing an offset voltage at the input which increases second harmonic distortion. This distortion therefore increases with input impedance (R//100kΩ in Figure 34), and with lower I_d values, as this increases the diodes' impedance. And, since the offset current is proportional to the transistor currents, second harmonic distortion will increase with larger I_{abc} values for a given input impedance.

Figure 35 shows the relative second and third harmonic distortion components for varying R values in the circuit of Figure 34. The input signal was varied in amplitude to cause the output current of the OTA to swing to $\pm$1/2 and $\pm$1/4 full scale, and the output distortion was measured for both cases. This was repeated for 1kΩ, 2.2kΩ, 5.6kΩ, 10kΩ, 22kΩ, 56kΩ, and 100kΩ. The results for 56kΩ were wildly variant from the rest of the values, and as such are not included in the graph (it's assumed an error in components, and not representative of actual circuit behavior). The source resistors of 100kΩ were held fixed for all tests.

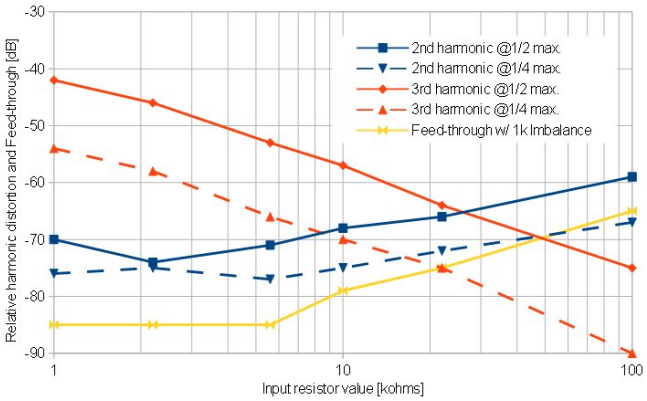

Fig. 35. Second and third harmonic distortion and feedthrough versus input resistance (R in Figure 34) for a fixed source resistor (100kΩ) and varying output levels ($\pm I_{abc}/4$ and $\pm I_{abc}/2$). Input trimmed for minimum feedthrough.

The second harmonic levels were down into the error range of the equipment (-75dB) for half of the range, rising around 10kΩ. The third harmonic distortion continued to fall for the entire range. To minimize overall distortion, operating around 10kΩ to 22kΩ input impedance would be best, which is coincidentally where the original tests were run for the single op-amp compensation scheme.

Figure 35 also shows CV feedthrough for the case where an extra 1kΩ imbalance is applied to the input. This can sometimes happen when the input to the OTA circuit is unbuffered, and the device it is connected to has a 1kΩ output protection resistor. This imbalance increases with the input resistor value (R). For small input resistances, the diode current will mostly go through the matched input resistors (R) and not the 100kΩ source resistors. But, as R approaches 100kΩ, the currents will be split more evenly, and this will increase the current going through the imbalanced 100kΩ resistors, and create a larger voltage difference at the OTA input. To minimize this imbalance and associated feedthrough, the input resistance should be kept much less than the source resistance (R $\leq$ 10kΩ in this case).

D. Optimal I_d and I_{abc} for minimal noise and distortion

There is a trade-off between SNR and distortion with increasing I_{abc}. Since the noise in the output transistors increases with $\sqrt{I_{abc}}$ and the output signal increases linearly with I_{abc}, the SNR is better at higher currents. But, as shown in Figure 36, this effect drops off around 150μA, where the noise begins to increase linearly as well, making SNR gains minimal. But, due to finite bulk emitter resistance in the LM13700 internal transistors, the distortion becomes worse at higher I_d and I_{abc}. This is due the fact that the distortion canceling effect of the linearizing diodes relies on the log-antilog relationship between these diodes and the input differential amplifier transistors. This effect is degraded by the increasing voltage drop across the bulk emitter resistance with higher currents.

A plot of log conformance error for the LM13700 transistors versus I_{abc} is shown in Figure 37. These data were taken from previous work using an LM13700 as a "thermal oven" exponential VCO core (see Addendum II of

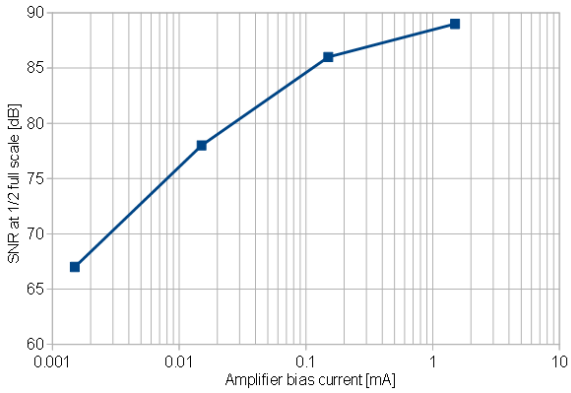

Fig. 36. OTA output SNR into 30kΩ load at 1/2 full scale signal ($\pm I_{abc}/2$) versus amplifier bias current (I_{abc}).

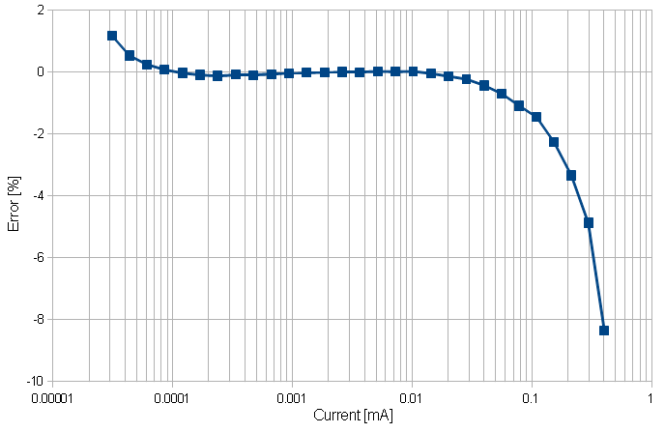

Fig. 37. Linearity of LM13700 transistors when used as an exponential converter (linearity error versus I_{abc}).

http://www.openmusiclabs.com/files/expotemp.pdf). The emitter resistance is quite high in the LM13700, and linearity begins to drop off precipitously around 50μA. It should be noted that this is the current through a single transistor, and both I_d and I_{abc} are split between two transistors, so currents of 100μA can be handled before reaching this level. From my experience i have seen a change of only a few dB in both SNR and THD when going from 100μA to 250μA, so any operating current in this range should be fine. Since the output noise is only a function of I_{abc}, running at a slightly higher I_{abc} than I_d can optimize this trade-off. For the most recent work done here with constant I_d schemes, an I_d of 100μA and an I_{abc} of 250μA were used.

E. Conclusions

The LM13700 can be used as a relatively low distortion and low noise multiplier, if other components are added. The improved dual OTA scheme makes this topology much more attractive than it was before, but it still requires the most parts of all the options, and a second trimmer (for second harmonic distortion) to take full advantage of its benefits. For lower cost designs, if there is a spare OTA, it is better used as a constant current source than in a dual OTA scheme.

When designing constant I_d OTA schemes, either with a single op-amp, external current mirror, or spare OTA, attention should be paid to the input resistance. The optimal resistance will be a function of I_d, I_{abc}, and the relative importance of second harmonic distortion, third harmonic distortion, and feedthrough increase due to source impedance imbalance. The distribution of the resistance between the source resistor (100kΩ here) and the input resistor (R) is a function of the input signal level and maximum output level. Lower output levels will give lower distortion, but at the cost of worse SNR.

Finally, there is very little benefit to operating the LM13700 above I_{abc} = 500μA. The SNR does not improve above this point, and distortion greatly increases. On the low end, distortion does not improve for currents less than 50μA, and SNR suffers below 100μA. The importance of this trade-off will depend heavily on the topology chosen. For single resistor compensation schemes, the distortion is not due to log conformance error and therefore current reduction does not help. For dual OTA schemes, the log conformance error is canceled out in the feedback loop, so current reduction also does not help. In these cases, operating at slightly higher currents is preferable. But, for the constant I_d schemes, small gains can be made by optimizing the I_d and I_{abc} currents.